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# RISC-V embedded AI for IDS applications

Pierre Garreau<sup>\*1</sup>, Pascal Cotret<sup>2</sup>, Jean-Christophe Cexus<sup>3</sup>, Julien Francq<sup>4</sup>, and Loïc Lagadec<sup>2</sup>

<sup>1</sup>Chair of Naval Cyber Defense – Ecole Navale – France

<sup>2</sup>Equipe Hardware ARchitectures and CAD tools – ENSTA Bretagne, Lab-STICC UMR CNRS 6285, Brest – France

<sup>3</sup>Equipe PIM – ENSTA Bretagne, Lab-STICC UMR CNRS 6285, Brest – France

<sup>4</sup>Naval Group – Naval Group – France

## Résumé

IDSs (Intrusion Detection Systems) include more and more AI (Artificial Intelligence) engines to detect several attack types. However, in order to be efficient in both learning and inference phases, such systems must include hardware coprocessors to improve AI-related computations. In this PhD thesis, we would like to explore the capabilities of RISC-V based processors in this context. RISC-V is an open-source ISA (Instruction Set Architecture) that can be easily extended. The main goal of this thesis is to propose RISC-V extensions for an IDS embedded into collaborative and heterogeneous unmanned vehicles (submarine, marine, or aerial): it must detect abnormal behaviors and must be efficient in terms of power consumption, area and runtime overheads. Furthermore, coprocessors developed in this thesis should not introduce security breaches into the system. Finally, a proof-of concept should be developed to demonstrate the efficiency of algorithms and hardware implementations compared to software solutions.

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\*Intervenant